Bunch by Bunch Feedback Processor Registers

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Detailed description of BBFP FPGA register map.

Mapping Overview

The FPGA register map runs from physical address 0x14000000 to 0x1403FFFF with the following assignments determined by the outer layer initially provided by Instrumentation Technologies:

CS	Start	End	Module
CS[0]	0x14000000	0x14003FFF	SBC Interface
CS[3]	0x1400C000	0x1400FFFF	System control
CS[6]	0x14018000	0x1401BFFF	History buffer control & data
CS[11]	0x1402C000	0x1402FFFF	TMBF control registers
	0x1403C000	0x1403FFFF	DAC clock control

Note that only the address ranges listed above are implemented. Address ranges corresponding to CS[1,2,4-5,7-10,12-15] are all unimplemented in the FPGA. The present document concentrates on the address area 0x14028000 to 0x1402FFFF documented below.

All registers are 32 bits wide. To obtain the register address from the given register number multiply the register number by 4 and add to the given base address.

Registers at 0x14000000

Only one register is available in this address space, for managing interrupt sources.

Reg	R/W	Bits	Register Description
0	R	31:0	Returns mask of currently active internal events.
	W	31:0	Sets the interrupt mask register, determines which internal events will raise an interrupt.

The following interrupt event source bits are defined:

Bit	Event Source
3	LMT events present, used for DDR buffer arm and trigger events
4	LMT half period
5	DDR buffer ready event

Registers at 0x1400C000

This block of registers interfaces to the clock control device through an SPI interface.

Reg	R/W	Bits	Register Description
0	RW	15:0	Write data to ADC Clock SPI register. Readback reads last value written.
1	RW	23:0	Write data to Clock Shift SPI register.
2	RW	0	Write 1 to enable clock domain, 0 to reset.

3	W	31:0	DCM control bits (to be determined)
	R	31:0	DCM controller readback value

Registers at 0x14018000

DDR history buffer control registers.

Reg	R/W	Bits	Register Description
0			(unused)
1	RW	23:0	Readout start address
2	RW	23:0	Readout step address
3	RW	23:0	Size of a single memory transfer
4	RW	23:0	Number of transfers to fetch, writing this register initiates transfer from DDR into FIFO
5	R	10:0	Number of words currently in FIFO
		30	Set if overrun detected
		31	Set if data busy
6	RW	31:0	SDRAM operation request, used for initialisation
7	RW	0	Enable or disable SDRAM. Write 0 to enable control
1024	R	31:0	Read advances FIFO

Note the FIFO advance register is at address 0x14019000.

Registers at 0x1402C000

The following register address space is part of the core DLS functionality.

The following registers based at address 0x1402C000 are used to control the TMBF processor. Note that only register 2 is both readable and writeable.

The following table shows a summary of the available 32 registers.

	Read	Write	
0	FPGA version and FIR tap count	Pulsed event register	
1	Status register	Write start and target selector	+
2		Control register #1	
3	Read latched pulsed events	Latch pulsed events	
4	DDR trigger point and capture count	Control register #2	
5		Detector bunch selection	*
6		ADC input offsets	*
7	Current super sequencer state	Super sequencer state count	
8		DAC pre-emphasis filter taps	*
9		ADC pre-emphasis filter taps	*
10			
11		Bunch zero offset	
12		DDR trigger delay	
13		BUF trigger delay	
14		Trigger blanking interval	
15			
16			
17		FIR coefficients	*
18		ADC minmax event threshold	
19		Bunch output configuration	*
20	ADC min/max		
21	DAC min/max		
22	Next word from BUF		
23		Sequencer configuration	*
24	Tune PLL status	Tune PLL configuration #1	
25	Tune PLL frequency FIFO	Tune PLL configuration #2	
26	Filtered detector IQ	Tune PLL integration factor	
27	Filtered NCO readback	Tune PLL configuration #3	
28	Min/max I	Tune PLL frequency offset limit	
29	Min/max Q	NCO setting	
30		Tune PLL proportional factor	
31		Readout control register	

+: Write to this register before writing to any register marked with *

***:** Repeated writes to this register, after initialisation by writing to register 1, write to blocks of internal setup state.

A more detailed description of each register follows:

Reg	R/W	Bits	Register Description
0	R	15:0	FPGA version
		19:16	Number of taps in FIR
	W		Pulse register. All writes to this register generate event pulses on the corresponding set bits.
		0	Arm DDR when written
		1	Soft trigger DDR when written
		2	Arm buffer and sequencer when written
		3	Soft trigger buffer and sequencer when written
		4	Arm bunch counter synchronisation when written
		5	Disarm DDR when written
		6	Disarm buffer and sequencer when written
		7	Interrupt sequencer and reset to state zero when written
		8	DDR capture enable
		9	Start ADC min/max readout
		10	Start DAC min/max readout
		11	Arm phase detect trigger
		12	Soft trigger tune following
		13	Start fast archiver buffer readout
		14	Arm triggered start of tune following
		15	Disarm triggered start of tune following
		16	Halt DDR capture when written
		17	Reset ADC minmax limit detection, pulsed after readout
		31:18	(unused)

1	R		Status register
		3:0	Sub clock phase bits at last trigger
		7:4	Sub clock phase bits when bunch clock synchronised
		12:8	DDR trigger source mask on last DDR trigger.
		15:13	BUF trigger source mask on last BUF trigger.
		18:16	Current sequencer state
		19	(unused)
		20	Set if buffer and sequencer waiting for trigger
		21	Set if buffer triggered and capturing data
		22	Set if sequencer busy and in non-zero state
		23	Set if DDR waiting for trigger
		24	ADC clock dropout detect. If set, FPGA must be reloaded to restore normal operation.
		25	Set if tune following start waiting for trigger
		26	Set if DDR data capture in progress.
		31:27	(unused)
	W		Write selector. Writing to this register initiates writing to FIR, bunch bank, and sequencer, and the written value determines the precise action.
		1:0	Bank selection for FIR and bunch bank writes.
		1:0	Sequencer write target: 0 for sequencer state memory, 1 for detector memory, 2 for sequencer offset memory.
		31:3	(unused)

2	W		Master control register
		0	DAC output enable
		1	Enable tune following feedback
		2	Detector input select, 0 for FIR, 1 for ADC
		5:3	Initial sequencer state
		6	Configure DDR for IQ or debug data capture
		7	Select sequencer start trigger source
		8	Write 1 to enable single bunch detector operation, 0 for multibunch detection.
		9	Select blanking source: external trigger or separate external SCLK input
		11:10	Buffer data select, one of: **0:** FIR + ADC **1:** Detector IQ data **2:** FIR + DAC **3:** ADC + DAC
		14:12	Define sequencer state to trigger DDC capture
		15	Select detailed tune following data for IQ buffer source.
		19:16	Fixed frequency HOM output gain in 6dB steps
		22:20	FIR output gain selection in 6dB steps
		23	Enable internal data loopback (testing only!)
		26:24	Detector readout gain selection in 6dB steps
		27	Front panel LED
		29:28	DDR input selection, together with bit 6, encoding as follows with bit 6 as the high bit: **0:** ADC **1:** FIR **2:** DAC before pre-emphasis **3:** DAC **4:** IQ **5:** Debug
		31:30	ADC input skew in 2ns steps

3	RW		Latch and readout pulsed events. To read out a bit it must first be latched (and reset) by writing the corresponding bit to this register before reading back this register.
		0	FIR overflow
		1	DAC output select and scaling overflow
		2	DAC pre-emphasis filter overflow
		3	ADC input overflow
		4	IQ FIR input overflow
		5	IQ accumulator overflow (very hard to trigger!)
		6	IQ detector readout scaling overflow
		7	ADC compensation filter overflow
		8	IQ FIR input overflow on DDR write
		9	IQ accumulator overflow on DDR write
		10	IQ detector readout scaling overflow on DDR write
		15:11	(unused)
		16	SCLK input event (or input high)
		17	Postmortem input event (or input high)
		18	Sequencer trigger event
		19	ADC min/max over limit event
		20	Trigger input event (or input high)
		31:21	(unused)
4	R	23:0	DDR trigger offset for DDR readout
	W		Secondary control register
		9:0	DAC output delay in 2ns steps
		11:10	(unused, reserved for extended DAC output delay)
		16:12	Enable DDR trigger sources, any bitwise combination of **0:** External trigger **1:** Postmortem trigger **2:** ADC limit overflow **3:** Sequencer state trigger **4:** External blanking signal trigger (SCLK)
		21:17	Enable blanking for corresponding DDR trigger source.
		23:22	ADC compensation filter group delay in 2ns steps
		26:24	Enable BUF trigger sources, any bitwise combination of **0:** External trigger **1:** ADC limit overflow **2:** External blanking signal trigger (SCLK)
		29:27	Enable blanking for corresponding BUF trigger source.
		31:30	DAC pre-emphasis filter group delay in 2ns steps

5	W	7:0	Channel bunch selection, written as four writes
6	W	16:0	ADC input offsets. Write to register 1 before writing four input offsets, one per ADC channel.
7	R	9:0	Current sequencer repeat number.
	W	9:0	Number of repeats of sequencer.
8	W	15:0	Taps for DAC pre-emphasis filter. Start by writing to register 1, then write 12 taps in order to this register. Write the same tap four times to fill the four banks.
9	W	15:0	Taps for ADC compensation filter. Start by writing to register 1, then write 12 taps in order to this register.
10			(unused)
11	W	7:0	Bunch zero offset when bunch trigger enabled
	W	23:16	Number of bunches-1 in machine
12	W	23:0	DDR trigger delay in turns after trigger
13	W	23:0	BUF trigger delay in turns after trigger
14	W	15:0	Trigger blanking interval in turns after trigger
15-16			(unused)
17	W	15:0	Write FIR coefficient. Initiate action by writing bank selection to register 1 then writing the correct number of taps.
18	W	15:0	ADC input threshold for ADC limit trigger
19	W		Bunch configuration. Initiate action by writing bank selection to register 1 then writing one config value for each bunch (936 values).
		10:0	Output gain for bunch
		13:11	Output selection for bunch, any sum of the following three bits: **1:** Output from FIR **2:** Output from fixed frequency NCO **4:** Output from swept NCO
		15:14	FIR bank selection for bunch.
20	R		Read out ADC min/max values since last readout
		15:0	Minimum ADC value since last readout
		31:16	Maximum ADC value since last readout
21	R		Read out DAC min/max values since last readout
		15:0	Minimum DAC value since last readout
		31:16	Maximum DAC value since last readout
22	R		Read next word from fast archiver buffer
		15:0	Low channel from archiver
		31:16	High channel from archiver
23	W	31:0	Writes to selected sequencer memory. See documentation below for details.

24	R		Tune following status. Bits 4:0 are accumulated between reads of this register and reset on read.
		0	Set if current integrated frequency deviation out of configured range.
		1	Set if current detected signal magnitude too small
		2	Set on detector output overflow
		3	Set on detector accumulator overflow
		4	Set on detector FIR input overflow
		5	Set if tune following feedback currently running
		7:6	(unused)
		12:8	Zero when feedback running, set to a copy of bits 4:0 at the point of feedback halting if feedback stopped.
	W	15:0	Tune following dwell time in turns
		16	Respect blanking signal and disable filter and processing while present. Stationary frequency updates are still generated.
		17	Enable multibunch detection on selected channel
		19:18	Select channel for detector
		27:20	Select bunch to detect in single bunch mode
		28	(Reserved for extended bunch selection)
25	R		Tune following frequency offset FIFO
		17:0	Tune following frequency offset
		30:21	Number of valid updates in buffer including current value, ignore bits 17:0 if this value is zero.
		31	Set if FIFO overrun has been detected
	W	17:0	Target phase for tune following feedback
		20:18	IIR scaling as a power of 2
		27:21	(unused)
		28	Input selection for tune following detector
		31:29	Detector output gain
26	R	15:0	Filtered I from detector
		31:16	Filtered Q from detector
	W	17:0	Feedback integral factor scaling
27	R	17:0	Filtered frequency offset from programmed NCO setting
		31	Set if NCO frequency includes frequency offset
	W	15:0	Minimum magnitude for feedback control
		18:16	IIR factor for IQ readback
		21:19	(unused)
		24:22	IIR factor for integrated frequency offset readback

28	R	15:0	Minimium I value since last reading
		31:16	Maximium I value since last reading
	W	16:0	Maximum frequency offset for feedback control
29	R	15:0	Minimium Q value since last reading
		31:16	Maximium Q value since last reading
	W	31:0	Fixed frequency NCO frequency, in phase advance per bunch, with 2^{32} corresponding to one revolution.
30	W	17:0	Feedback proportional factor scaling
31	W		Readout control register
		0	Write this bit to latch the current accumulated status
		2:1	Write these bits to latch the accumulated min/max I&Q.

Sequencer Memory

The sequencer memory is written to by first selecting the memory area by writing the appropriate selection to register 1 and then by writing the appropriate number of words to register 23. There are three areas of memory.

Sequencer state memory:

The sequencer state momory is selected by writing 0 to register 1.

The sequencer state consists of 8 lines (one for each programmable state), each state is written by writing 8 words, so a total of 64 words should be written to update the sequencer state. Each state line consists of the following 8 words.

Reg	Bits	Register Description
0	31:0	Sweep start frequency in phase advance per tick
1	31:0	Sweep step frequency in phase advance per tick
2	15:0	Sweep dwell time in turns (add 1 for actual count)
3	11:0	Sweep capture count (add 1 for actual count)
	13:12	Bunch bank selection
	17:14	Swept NCO output gain in 6dB steps
	18	Enable detector window
	19	Enable sweep detection and writing to buffer
	20	Observe trigger blanking pulse during acquisition
	31:21	(unused)
4	31:0	Detector window advance per turn. Program so that dwell time * 234 * window advance is close to 2^{32}.
5	15:0	Sweep capture holdoff
	31:16	(unused)
6-7		(unused)

Detector window memory:

The detector window memory is selected by writing 1 to register 1.

The detector window consists of 1024 signed 32-bit numbers which are used to window the input data into the detector.

Super sequencer offset memory:

The offset memory is selected by writing 2 to register 1.

The offset memory consists of frequency offsets that are added to the sequencer sweep frequencies as the super sequencer steps.

Tune Following Data

When tune following detail data has been selected (by setting bit 15 of control register 2) and IQ data has been selected for the buffer, the buffer contains the following data.

Channel	Bits	Data Description
0	15:0	I data from decoder
	31:16	Q data from decoder
1	15:0	Magnitude from I/Q, scaled by CORDIC adjustment factor
	31:16	Angle decoded from I/Q (top 16 bits of 18 bits)
2	17:0	Filtered angle with reference angle subtracted, used as error term for feedback control
3	17:0	Final frequency offset out
	22:18	Snapshot of current status
	23	Running bit
	28:24	Stop reason status bits
	29	Set if holdoff active

External LEDs

There is an LED on the front panel, and there are three LEDs on the rear panel. The rear LEDs are numbered from left to right in the table below.

Front panel LED

This LED is under software control through control register bit 27.

Rear panel LED #1

This LED shows the SBC clock divided down by 2^{25}, so flashes at just under 4Hz.

Rear panel LED #2

This LED shows the status of the ADC clock. If on, the ADC clock is ok, if off there has been a glitch in the ADC clock as reported through status register bit 24.

Rear panel LED #3

This flashes on for around 60ms on each trigger.

Registers at 0x1403C000

This part of the address space is recognised by hardware external to the FPGA.